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Development of Parametric Material, Energy, and Emission Inventories for Wafer Fabrication in the Semiconductor Industry

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Currently available data suggest that most of the energy and material consumption related to the production of an integrated circuit is due to the wafer fabrication process. The complexity of wafer manufacturing, requiring hundreds of steps that vary from product to product and from facility to facility and which change every few years, has discouraged the development of material, energy, and emission inventory modules for the purpose of insertion into life cycle assessments. To address this difficulty, a flexible, process-based system for estimating material requirements, energy requirements, and emissions in wafer fabrication has been developed. The method accounts for mass and energy use at the unit operation level. Parametric unit operation modules have been developed that can be used to predict changes in inventory as the result of changes in product design, equipment selection, or process flow. A case study of the application of the modules is given for energy consumption, but a similar methodology can be used for materials, individually or aggregated.

Introduction

Semiconductor devices are manufactured or fabricated on round disks of crystalline silicon (wafers) in a process called wafer fabrication. Wafers range in size from 4 in. (100 mm) to 12 in. (300 mm) in diameter and contain hundreds of individual semiconductor devices or die. Most production wafers are 8 in. (200 mm). In 2002, there were 65.9 million (10^6) 8-in. wafer equivalents processed worldwide (*1*). Assuming electricity consumption of 1.4 kW-h/cm^2, water use of 5.9 L/cm^2 (*2*), and a wafer area of 314 cm^2, this results in an estimated 2.9×10^{10} kW-h of electricity and 1.2×10^{11} L of water used annually in wafer fabrication. The energy and material use associated this portion of the semiconductor industry is clearly substantial; therefore, application of green engineering principles to the process of wafer fabrication could potentially lead to both cost savings and environmental benefit. In particular, the fourth principle of green engineering states that products, processes, and systems should be designed to maximize mass, energy, space, and time efficiency (*3*).

While wafer fabrication, as used in the manufacture of semiconductor devices, is resource-intensive using large amounts of energy, water, and chemicals (*4, 5*), the inventories associated with this activity are poorly understood and not well-documented (*6*). Reverse engineering of the silicon chip reveals little about how it was manufactured, as most of the materials used in the manufacturing process never reside on the wafer or are later removed. In addition, process flows (the sequence of unit operations and chemical recipes for manufacturing the wafer) are complex and change rapidly. A single wafer fabrication facility may manufacture hundreds of products, and the development of separate product-based inventories for each could be extremely difficult and time-consuming. Product lifetimes are typically less than 2 yr, which raises the concern that in the time that it takes to develop an accurate inventory, the data will no longer be valid. It is also difficult to perform tradeoff analyses and predict how changes in product or process design (including equipment selection) will affect the inventory.

Systems used to develop material and energy inventories for complex and rapidly changing products and processes such as semiconductor wafers must therefore be flexible and may need to rely on obtaining the maximum amount of information with limited data. The methodology described in this work uses process-based, generic, parametric modules for process flows associated with wafer manufacturing. The long-term goal of this effort is to develop generic material use, energy use, and emission inventories that can be applied to multiple facilities in the absence of site specific information (*7*).

Individual semiconductor manufacturers have previously attempted to develop process-based inventory modules by either assembling facility-wide data, and then assigning fractions of the inventory to specific processes (top-down approach) (*8*) or aggregating data obtained from individual pieces of equipment used in a process (bottom-up approach) (*9*). Neither has proved satisfactory to the majority of practitioners within the industry (*6, 10*). The top-down approach, while providing a rapid and accurate measure of current or recent mass and energy flows, is not conducive to assigning inventories to individual processes or products for the purpose of differentiation and/or improvement. The bottom-up approach has the potential to be extremely precise but is very time-consuming and potentially inaccurate as it risks missing the effects of macrovariables associated with idle time, test and maintenance runs, and interactions with other activities.

An alternative is to organize the inventory around the unit operations associated with wafer fabrication using data collected at both factory and equipment levels. Organizing the inventory around unit operations has several advantages. Most wafer manufacturing lines are structured along similar lines, thus facilitating the creation of generic modules that have applicability in multiple facilities. Unit operation modules can be repeated and pieced together as building blocks that describe an overall process flow even if the degree of certainty within the individual blocks varies. This approach also takes advantage of the fact that while the products and the materials and equipment used to generate semiconductor devices are being constantly updated and the "recipes" that the equipment uses change, the basic unit operations remain relatively stable. Thus, a "typical" mass and energy flow can be developed for each unit with the opportunity to add detail as available and needed. Relationships can be defined between inventory and product design features (e.g., film thickness) and process characteristics (e.g., deposition tem-

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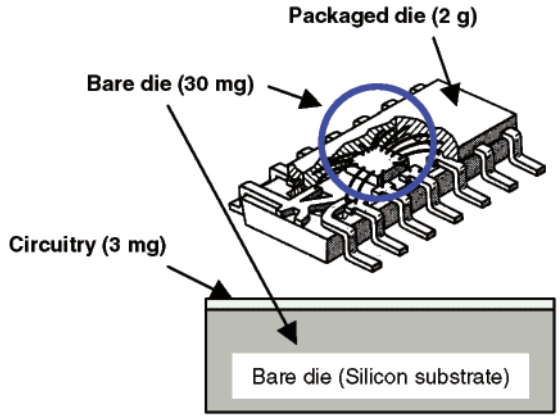

FIGURE 1. 2-g packaged die contains a bare die that weighs about 30 mg upon which is about 3 mg of active semiconductor circuitry.

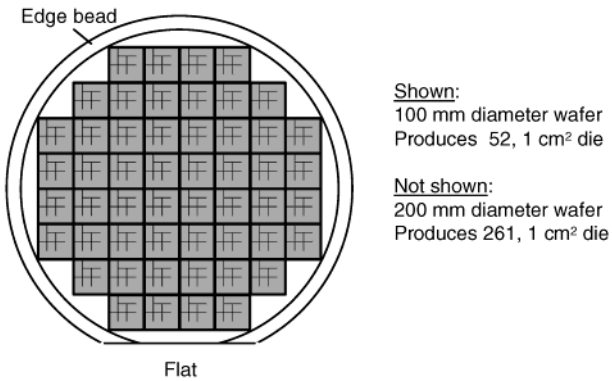

FIGURE 2. Rectangular die patterned on a round silicon disk referred to as a wafer.

perature). Other relationships can be characterized for variables such as equipment type (e.g., horizontal vs vertical furnace). The goal is to identify key variables that can be defined in way that is relatively independent of a particular product but which affect the inventory in a predictable and quantifiable manner.

Given the difficulties associated with direct measurement, the resultant estimated values for a process may be more accurate than those derived from detailed equipment-level data. A parametric approach also facilitates the development of predictive life cycle assessments for emerging technologies at both the product and the process design stages. Additional information regarding unit operations and their use in generating wafer fabrication inventory modules is available in related publications (*6*, *7*). In addition to the actual manufacturing line, semiconductor wafer fabrication requires a complex facility that generates, manages, and delivers inputs to the line (ultrapure water, air, and chemicals) and that collects and treats outputs (wastes). The *International Technology Roadmap for Semiconductor Technology* estimates that the resource demands in terms of chemical, water, and energy usage are roughly equal between facilities (or infrastructure) and the manufacturing line (wafer fabrication) (*11*). However, these are based on very rough estimates and often old data (*12*). This is clearly an area that requires additional study. While the current work is focused solely on the manufacturing line, it is anticipated that a similar methodology could be employed for the infrastructure unit operations as well.

Wafer Fabrication Processes

The term semiconductor device or microchip, when applied to a product, refers to the "packaged die" or component that is attached to a printed wiring board. Each component is small (most are 2 cm on a side or less) but enclosed within it is a much smaller "bare die" upon which the actual semiconductor device is built. The bulk of the visible component consists of a protective plastic package and the metal wires and leads required to create electrical connection between the bare die and the printed wiring board. The enclosed bare (unpackaged) die are commonly 3−12 mm on a side and range in thickness from 100 to 500 μm. However, only the top portion (10−20 μm) of the die is actually functional circuitry (Figure 1). This means that a 2-g packaged die or microchip contains about 3 mg of active semiconductor devices. Williams et al. (*4*) estimated that the total weight of secondary fossil fuel and chemical inputs to produce a single 2-g 32MB DRAM packaged die was 1272 g, or more than 600 times the weight of the final product. However, almost all of this is used for the creation of a 30-mg die with 3 mg of active semiconductor circuitry, which equates to more than 40 000 or 400 000 times the weight of these more fundamental portions of the product, respectively.

Semiconductor devices are created using a sequence of unit operations that result in selectively "doped" regions of silicon and etched thin films. The basic unit operations used in manufacturing are chemical vapor deposition (CVD), furnace operations, metallization, wafer clean, ion implant, chemical mechanical polishing (CMP), photolithography, and etch. While often further subdivided, these eight operations are generally recognized and understood across the industry and are therefore useful in the creation of generic modules describing wafer fabrication.

A wafer can be thought of as patterned layers of circuitry and insulation built one on top of the other, with each layer defined using a unit operation called photolithography. In photolithography, an organic resist is patterned by selective exposure through a mask (similar to a photographic negative) using ultraviolet (UV) light. For each layer of circuitry or insulation, the pattern is "stepped" or repeated many times across the wafer in order to produce multiple die (Figure 2). The size (measured as diameter) of the wafers varies, primarily based on the age of the wafer fabrication facility. There are a small number of 4-in. (or 100-mm) facilities; equipment at these sites would be about 15−20 yr old. Beginning in the late 1980s, equipment to support the manufacture of 6-in. or 150-mm facilities became available. Most factories built since the mid- to late-1990s have been equipped to handle 8-in. or 200-mm wafers. Technical capabilities at different wafer fabrication facilities are strongly correlated with age and therefore wafer size.

Most semiconductor products are manufactured using between 15 and 25 mask layers. In general, the processes used are sacrificial, subtractive, and/or have extremely low material utilization efficiencies (defined as the fraction of the material used to that incorporated into the final product). A blanket film is typically deposited uniformly across the wafer. However for many layers, the bulk of the material is not desired in the final product; hence, the film is typically covered with a patterned resist and 50−100% of the film removed (i.e., subtracted or sacrificed) at subsequent unit operations (photolithography and etch). In addition, the processes themselves may require significantly more material than actually ends up on the wafer. In growing an oxide film, for example, it is estimated that only 0.05% of the oxygen gas used in the process is incorporated into the product.

Because the size of the individual features on the die is exceedingly small (less than 1 μm), the surface must be kept free of all physical and chemical contamination. This requires that the wafers be thoroughly cleaned before each layer is created. An illustration of how one layer is created is given in Figure 3.

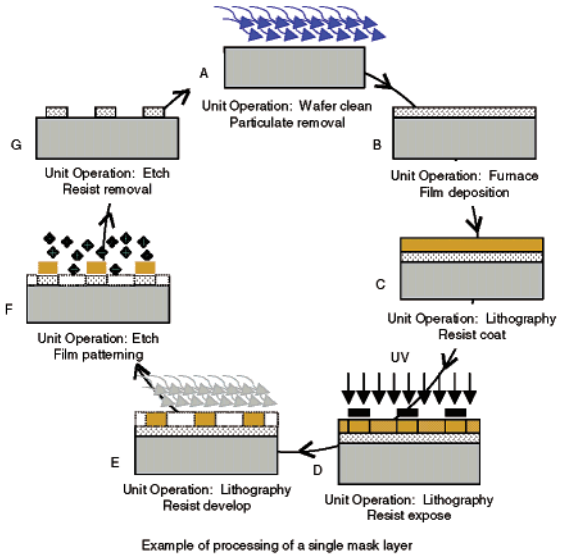

FIGURE 3. Single mask layer illustrated involves four unit operations (wafer clean, furnace, photolithography, and etch) and seven functions (particulate removal, film deposition, resist coat, resist expose, resist develop, film patterning, and resist removal). Between 15 and 25 such cycles are commonly used in wafer fabrication.

Current Inventories

Semiconductor manufacturers are very aware of the volume of materials that they consume as well as the associated emissions and waste (*2*), and there have been significant levels of effort within the commercial sector to reduce both material and energy demands. Nevertheless, the focus within the manufacturing environment has been and is likely to continue to be on maintaining leading-edge technologies and controlling costs. In addition, there are concerns that detailed collection of inventory data will disrupt manufacturing flows. As a means to overcoming these barriers, many major semiconductor manufacturing corporations are working in close cooperation with several governmental, academic, and nonprofit entities that are trying to address environmental concerns related to wafer fabrication. The National Science Foundation in conjunction with the Semiconductor Research Corporation (SRC) has established an Engineering Research Center for Environmentally Benign Semiconductor Manufacturing at the University of Arizona (*13*). One of the major thrusts at International SEMATECH (ISMT) (*14*), a consortium of major semiconductor companies, has been environment, health, and safety. However, while there are some efforts within these organizations to examine direct material and energy consumption during wafer fabrication, the majority of the projects have emphasized either upstream concerns (water purification) or downstream issues such as copper-bearing slurry waste from chemical mechanical polish (CMP) and perfluorocompounds (PFC emissions). Consequently, the industry is still in need of inventory data and/or a means to accurately estimate values for the purpose of providing input to life cycle analyses specifically for wafer fabrication. There is also a desire to have information about material and energy consumption during the design phase (product and process) in order to control both cost and environmental burden.

A small number of life cycle assessments for wafer fabrication have been performed (for a summary and literature review, see ref *6*). Of the two most detailed studies, one included wafer fabrication as part of the analysis of the manufacturing and use of an EPROM (erasable programmable read-only memory) device; in this case the packaged die was the functional unit (*15*). The second analysis included only wafer fabrication within the system boundaries and used a wafer as the functional unit, but data were gathered from a facility that is known to be using old technology (*16*). Other sources of inventory data are available in Williams et al. (*4*), in the Microelectronics and Computer Technology Corporation Roadmap (*5*), and in the SIA roadmaps (*2*, *11*, *17*, *18*). These are all based on highly aggregated data with little process-specific information. In addition, the data are derived from single product types and/or specific equipment and process approaches that may or may not be generally applicable to other facilities, especially of varying age. None of the available data from actual manufacturing sites represent modern facilities fabricating 200-mm wafers. The SIA roadmap data (*2*, *11*, *17*, *18*) are for cutting-edge technology and based on targeted values rather than actual data. In both cases, the numbers are probably not representative of roughly half of the facilities in operation today.

TABLE 1. Top 25 Materials for Which Improved Inventory Is Desired by ISMT Member Companies

name	CAS Registry No.
sulfuric acid (H_2SO_4)	7664-93-9
isopropyl alcohol ($(CH_3)_2CHOH$)	67-63-0
phosphoric acid (H_3PO_4)	7664-38-2
hydrochloric acid (HCl)	7647-01-0
tetramethylammonium hydroxide ($(CH_3)_4NH_4$)	75-59-2
nitric acid (HNO_3)	7697-37-2
hydrofluoric acid (HF)	7664-39-3
hydrogen peroxide (H_2O_2)	7722-84-1
N-methyl pyrrolidone (C_5H_9NO)	872-50-4
nitrogen trifluoride (NF_3)	7783-54-2
ammonium fluoride (NH_4F)	12125-01-8
ammonium hydroxide (NH_4OH)	1336-21-6
butyl acetate ($CH_3COO(CH_2)_3CH_3$)	123-86-4
ethyl lactate ($C_5H_{10}O_3$)	97-64-3
hexamethyl disilazane ($C_6H_{19}NSi_2$)	999-97-3
silica, amorphous (SiO_2)	112945-52-5
sodium hydroxide (NaOH)	1310-73-2
propylene glycol monomethyl ether acetate ($C_6H_{12}O_3/CH_3CH(OCOCH_3)CH_2OCH_3$)	108-65-6
acetic acid (CH_3COOH)	64-19-7
water	7732-18-5
photo resists	–
energy	–
ACT-690c ($H_2N(CH_2)_2OH$)	141-43-5
acetone (CH_3COCH_3)	67-64-1

A ranking of materials based on the need for improved inventory/use data as inputs to life cycle analyses was made by member companies of ISMT and is presented in Table 1 (*6*). Note that all of the top 20 are considered specialty chemicals, with the primary concern being toxicity and material and energy consumption related to upstream manufacture of the chemicals. This suggests that a life cycle approach (*19*–*21*) for assessing these material flows should be employed. However, from the perspective of developing an inventory for wafer fabrication, it is less clear that these should be the materials of interest. First, the consumption of these materials is relatively well-known because they are expensive (1 L of resist may cost as much as $500) and are typically tied to specific operations.

Second, if the four broad areas of consumption for wafer fabrication are considered (energy, water, elemental gases, and specialty chemicals), specialty chemicals represent by far the smallest fraction of mass utilized (Figure 4). This is not to imply that developing inventories for these materials is not needed, but rather that the other three categories have tended to receive less attention despite their significant contribution to the environmental load and therefore represent a larger information gap. In addition, while the per unit costs are low, the total costs of energy, water, and

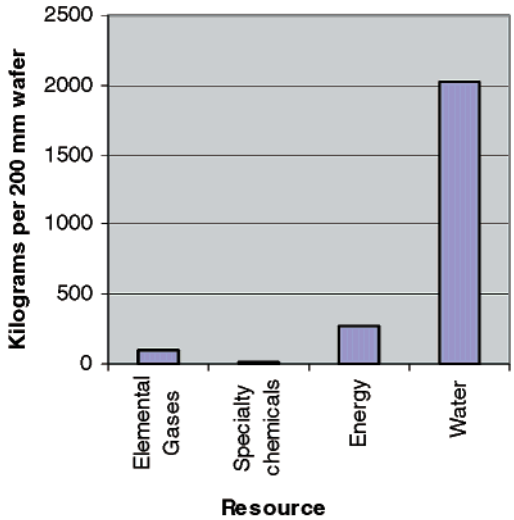

FIGURE 4. Energy and water account for the largest fraction of material consumption in the wafer fabrication process. Data are derived from Williams et al. (*4*) and SIA (*2*).

elemental gases can be significant. For example, on a wafer with 20 mask layers using resist at $125/L (more likely than the extreme of $500/L cited above) and 4 mL/layer, the resists contributes $10 to the total cost. In contrast, energy at 300 kW-h/wafer and $0.06/kW-h contributes $18 to the total cost.

Based on the data in Figure 4, it is clear that an assessment of the material use, energy use, and emissions associated with wafer production must include not only specialty chemicals but also water, energy, and elemental gas use. While according to Table 1, the industry ranks water 21, energy 23, and nitrogen and oxygen 40 (not shown and tied with 48 others), the importance of these should not be underestimated. From an inventory perspective, they represent many orders of magnitude greater mass flow than the specialty chemicals. Furthermore, although overall usage at a particular site is generally known, it is often difficult to associate flows with specific operations. This limits the ability to effectively control or reduce consumption and makes any type of activity-based analysis (whether for the purpose of cost or environmental improvement) quite difficult. Finally, although the intent of this work is to address the inventory directly associated with wafer fabrication processes, if the final goal is to insert this inventory into a full life cycle assessment, the high-purity requirements for water and gases must be considered, as these require significant upstream energy and material investments.

There are several barriers to direct measurement of water, elemental gases, and energy consumption during wafer fabrication. Determining the power draws on equipment in a factory environment may require taking a piece of equipment off-line, which is often not practical. Water and nitrogen are used ubiquitously throughout the manufacturing facility, and typically there are no means for monitoring their use at a particular location or unit operation. Therefore, development of modules that permit prediction of energy and material consumption as function of product and process design rather than requiring direct measurement would be extremely useful. In the examples given below, the modules are developed based on process recipes and equipment specifications rather than direct measurement of mass and energy during production runs. Yet, with validation through a small number of direct off-line measurements and equipment calibrations (such as on mass flow controllers), these models are expected to be quite accurate.

Parametric Module Development

The goal of the work presented in this paper is to develop methods for estimating material requirements, energy requirements, and emissions for wafer fabrication that can be applied to a variety of product and process configurations. The methodology is demonstrated for consumption of energy and one elemental gas (O_2); however, the approach can be applied to all material categories and emissions. The database from which these modules were developed is discussed later in this document.

The following definitions are used in describing the development of the modules. A recipe is a list of processing steps defined for a particular piece of equipment; it is typically programmed into a computer that is integral to the equipment. The recipe defines a stepwise process and sets the process parameters for each step such as time, temperature, and material flows.

A "function" is defined by the functionality that is added to the devices on the wafer. For example, "gate oxide" describes the function where a thin layer of silicon dioxide is grown by oxidizing silicon at elevated temperature in an atmosphere of oxygen (O_2). Different product specifications may call for different thickness and therefore different recipes.

"Equipment type" is used to describe different equipment designs that can be used to perform the same function. Silicon dioxide may be grown in a horizontal furnace (axis parallel to the ground), in a vertical furnace (axis perpendicular to the ground), or in a rapid thermal processor (RTP), which uses infrared lamps to provide thermal energy. In some cases, not all functions can be performed on all equipment types. RTP, for example, is limited to the formation of layers of a few hundred angstroms or less while horizontal and vertical furnaces can be used to grow or deposit layers that are several thousand angstroms thick.

The "unit operation" includes one or more equipment types and is generally defined by the intersection of equipment characteristics and process requirements. The furnace unit operation, for example, is used to impart thin insulating layers of silicon, silicon dioxide, or silicon nitride on the wafer (process requirements) through the use of heat and gas flows (equipment characteristics). In some cases, the unit operation is composed of tightly linked subunit operations. These subunit operations use a different type of equipment and/or impart a different functionality to the wafer, but because they are integral to the primary function, they are included in the overall unit operation description. In the photolithography unit operation, for example, wafers must first be coated, then exposed, and last developed (Figure 3). This requires different types of equipment (a track for coat and develop and a stepper for expose), but because one operation is never done without the other and because the equipment is linked, they are generally included in a single unit operation. The hierarchical relationship between the levels described in the preceding paragraphs is shown in Figure 5.

Finally the "process flow" is defined by the specific combination of unit operations that are determined as a function of product specifications. A wafer will go through each of the eight unit operations multiple times; each time it passes from one unit operation to the next, it is said to have completed a process step. The full process flow for a wafer typically includes a minimum of 50 and sometime hundreds of process steps (Figure 6).

Using the organization concepts described above, four types of modules have been developed: modules based on product specifications at the function level, modules based on equipment design at the equipment level, modules based on equipment type and processing parameters at the unit operation level, and modules based on the number of unit operations performed at the process flow level.

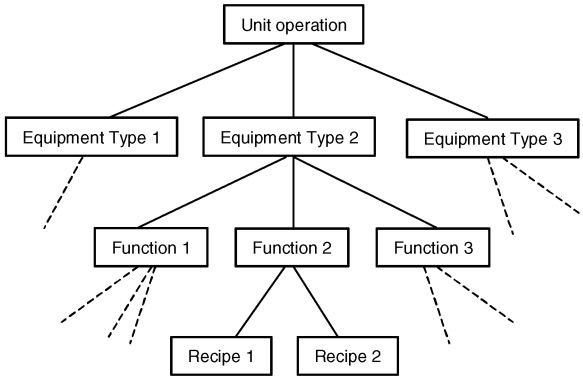

FIGURE 5. Tree structure used to illustrate the relationship between the levels at which parametric modules can be developed. Parametric modules are developed at the function level using recipe parameters and at the unit operation level using either equipment type or function parameters.

Wafer Process Flow

Step 1	Unit operation – wafer clean
Step 2	Unit operation – furnace
Step 3	Unit operation – wafer clean
Step 4	Unit operation – lithography
Step 5	Unit operation – implant
Step 6	Unit operation – etch (ash)
Step 8	Unit operation – wafer clean
Step 9	Unit operation – furnace
Step 10	Unit operation – lithography
Step …	Unit operation – ……..
Step n	Unit operation – etch (ash)

FIGURE 6. Wafer process flow consists of 50 to hundreds of steps as it is repeatedly processed through each of the eight unit operations in varying sequences.

Modules at the Function Level. Modules at the function level describe material and energy use for different product specifications, such as film thickness. As an example, consider the energy and oxygen requirements associated with growing an oxide layer in the function "copper oxide" within the furnace unit operation. Different products or different layers within the same product might be designed with a different thickness, yet the oxide is grown with the same basic recipe and equipment. Oxygen consumption and energy use data were collected from different recipes used to form a range of oxide layer thicknesses, using methods described in the database section of the paper. Figures 7 and 8 show the data.

Figure 7 shows the empirical parametric relationship between thickness and energy consumption. The parametrization can be used to estimate energy consumption for a continuum of oxide layer thicknesses, ranging between 2500 and 6300 Å. To a limited degree, it may also be possible to extrapolate beyond the defined range. This same approach can be used to develop a parametric module for the volume of oxygen used (Figure 8) and for hydrogen consumption (not shown) for the same thermal oxide function. Note that nitrogen, which is also used in the function, is not dependent upon thickness; consequently, the volume consumed is the

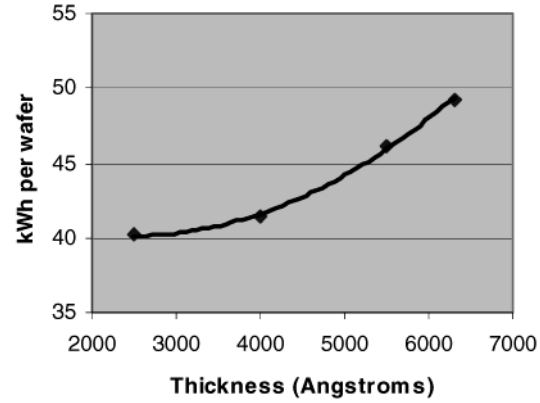

FIGURE 7. Energy consumption per 8-in. wafer as a function of layer thickness shown for thermal oxide grown in a horizontal furnace in the presence of hydrogen (wet oxidation). The empirically derived relationship is kW-h/wafer = $(6.0 \times 10^{-7} \bullet \text{thickness}^2\ (\text{Å}^2)) - (3.1 \times 10^{-3} \bullet \text{thickness}\ (\text{Å})) + 44$, with a correlation coefficient (R^2) of 0.998.

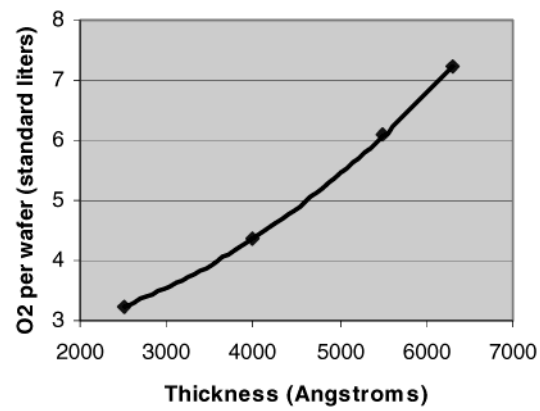

FIGURE 8. Oxygen (O_2) consumption per 8-in. wafer as a function of layer thickness for thermal oxide grown in a horizontal furnace in the presence of hydrogen (wet oxidation). The empirically derived relationship is O_2 (standard L)/wafer = $1.0 \times 10^{-7} \bullet \text{thickness}^2\ (\text{Å}^2)) - (9.0 \times 10^{-5} \bullet \text{thickness}\ (\text{Å})) + 2.6$, with a correlation coefficient (R^2) of 1.

same for all four thicknesses. The nonlinear nature of these relationships is due to diffusion effects (i.e., as the film thickness increases it takes longer for the oxygen to diffuse through the newly created oxide layer to reach the oxide silicon boundary).

Modules at the Equipment Level. Discrete rather than continuous relationships are often the basis for module development at the equipment level. These inventory modules can be used to perform tradeoff analyses between equipment designs, assuming that the same function is performed on each system. Wafer cleaning occurs before almost every process step and accounts for a significant amount of chemical usage and the majority of the water use in wafer fabrication. This unit operation also exhibits relatively little variation from company to company and is therefore easy to characterize. A comparison of the material consumption in four different wafer clean equipment types using one of the most common cleaning chemistries is presented by Murphy et al. (*7*). This type of module results in discrete parametric relationships, best represented in tabular rather than graphical form.

Modules at the Unit Operation Level. A third type of parametric module is one developed based on unit operation design. As a first example, consider the effects of equipment selection on energy consumption in furnaces creating oxide layers. In comparing the environmental metrics associated

with different types of equipment, it is often straightforward to compare the results on the basis of "per unit processed," also referred to as a "wafer pass". While this is conceptually simple, in practice, it must be recognized that wafer fabrication unit operations are not operated continuously but rather in lots of 25 or 50 wafers. Material and energy consumption during the time between lot runs is often a significant fraction of total material and energy use. In particular, furnaces are rarely shut down between runs but are operated in an idle mode at or near process temperature. Therefore, to properly account for process material and energy consumption on a per wafer basis, it is necessary to account for both the active and the idle characteristics of the process.

The following example illustrates the importance of characterizing idle times in developing material and energy inventories for unit operations. In this example, the process energy consumption is parametrized against production level in units of wafers processed per week.

To grow a thin layer (25 Å) of silicon dioxide (SiO_2) in the furnace unit operation, two equipment options are considered: a vertical furnace and a rapid thermal processor (RTP). The vertical furnace processes a batch of up to 150 wafers in about 4 h, which equates to 0.0262 h/wafer. In contrast, the RTP process takes just over 3 min, but only one wafer is processed a time at 0.162 h/wafer. For both pieces of equipment, it is assumed that they are left at or just below process temperature while in the idle mode.

Power draws for both process and idle modes can be measured directly (*22*) and are used in this analysis, or alternatively they may be estimated as a percentage of the design value of the equipment as specified by the equipment supplier. Measurements taken on equipment at ISMT indicate that power requirements for the RTP are 48 kW during processing and 45 kW during idle. The vertical furnace requirements are 21 and 16 kW for processing and idle, respectively.

A semiconductor manufacturer would make the following types of calculations using numbers specific to its facility. In this example, a hypothetical wafer fabrication facility (fab) is modeled based on the assumption that the facility is operating 24 h a day, 7 days a week, with 80% production time, which equates to 134 production hours per week. The number of wafer starts per week is set at 5000.

The total equipment demand time in hours per week for a given function is calculated as given by

$$\text{time}_{\text{equip demand}} = \frac{(\text{wafers/week})(\text{h/run})}{\text{wafers/run}} \qquad (1)$$

Using eq 1, the total equipment demand time ($\text{time}_{\text{equip demand}}$) required for the vertical furnace to grow 25 Å of gate oxide on 5000 wafers is

$$131\ \text{h/week} = \frac{(5000\ \text{wafers/week})(3.92\ \text{h/run})}{150\ \text{wafers/run}}$$

Similarly, the total equipment demand time ($\text{time}_{\text{equip demand}}$) for the RTP is

$$810\ \text{h/week} = \frac{(5000\ \text{wafers/week})(0.162\ \text{h/run})}{1\ \text{wafer/run}}$$

This indicates that multiple RTPs are required to support the desired throughput. The number of units needed is calculated using

$$\text{units}_{\text{equip}} = \text{roundup}\ [(\text{time}_{\text{equip demand}})/\text{time}_{\text{prod}}] \qquad (2)$$

Assuming that production time ($\text{time}_{\text{prod}}$) is 134 h/week, the total number of RTP units required is

$$7\ \text{units} = \text{roundup}\ [(810\ \text{h/week})/(134\ \text{h/week})]$$

Idle time is calculated by subtracting equipment demand time ($\text{time}_{\text{equip demand}}$) from the total available equipment hours or equipment available time per week, which is equal to the number of equipment units ($\text{units}_{\text{equip}}$) multiplied by production time ($\text{time}_{\text{prod}}$) as given by

$$\text{time}_{\text{idle}} = (\text{units}_{\text{equip}} \times \text{time}_{\text{prod}}) - \text{time}_{\text{equip demand}} \qquad (3)$$

For the RTP at 5000 wafers/week, this equates to

$$128\ \text{h/week} = (7\ \text{units} \times 134\ \text{h/week}) - 810\ \text{h/week}$$

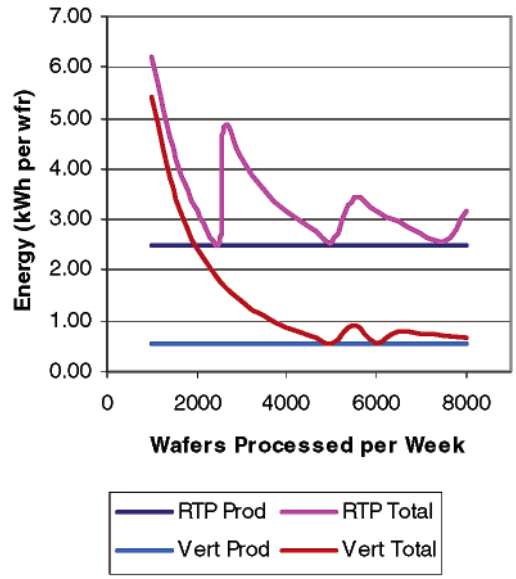

FIGURE 9. Energy consumption for growth of a 25-Å oxide layer as a function of equipment type (RTP vs vertical furnace), number of wafers processed per week, and total run time (production plus idle). The example shown is for 8-in. wafers.

To understand the effects of equipment idle time on total energy consumption for the unit operation, the above calculations were done for a continuum of production levels from 1000 to 8000 wafers/week. The results are presented in Figure 9. In all cases, for both pieces of equipment, the total energy demands are higher than would be predicted if only the process mode were accounted for. Also, if only process mode were considered, it would be assumed that the energy demands of the RTP were always about 5 times greater than that of the vertical furnace. However, if the effects of running in the idle mode are considered, the energy demands of the RTP and vertical furnace are very similar at less than 2500 wafers/week.

Figure 9 illustrates that an increase in the number of required pieces of equipment to meet capacity can result in excess idle time, which is evident in the peaks of the total energy curves for both pieces of equipment. Note that although the energy demands of the RTP are generally higher than the vertical furnace, if use of the RTP increases yield by any significant amount, then the increase in energy consumption by this one layer would be more than off-set by a decrease in scrap since scrapping a wafer implies losing all of the energy invested in its processing up to the point at which it is scrapped.

As an example of a module at the unit operation level based on process design, consider the effects of temperature on oxygen (O_2) consumption. Silicon dioxide is grown in the furnace unit operation by flowing oxygen over bare silicon

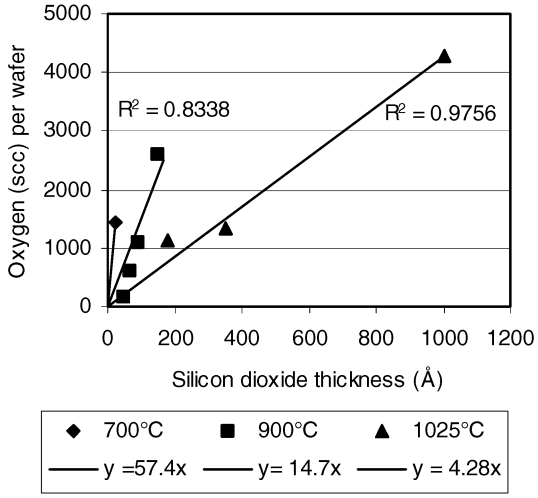

FIGURE 10. Oxygen (O_2) consumption per 8-in. wafer as a function of silicon dioxide thickness and temperature for thermal oxide grown in a vertical furnace using dry oxidation (no hydrogen present).

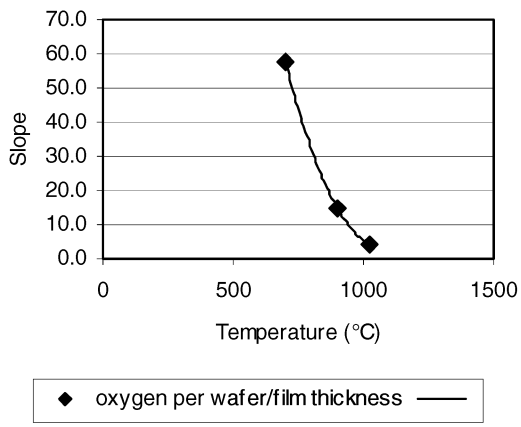

FIGURE 11. Slope of oxygen consumption curves determined as a function of film thickness and process temperature for an 8-in. wafer.

at temperatures between 700 and 1050 °C. Higher temperatures are typically used for thicker layers in order to accelerate the process. Lower temperatures are used for thinner layers in order to maintain thickness control. There is, however, some overlap between the thickness ranges grown at various temperatures.

Eight different oxidation recipes from four different functions within the furnace unit operation were used to examine the effects of temperature on oxygen consumption. The three different temperatures represented within the eight recipes were plotted against oxygen consumption as a function of oxide layer thickness (Figure 10). The resulting slopes were then plotted as a function of temperature, and a best-fit polynomial equation was generated (Figure 11).

The final predictive equation is

$$O_2 = (0.0004T^2 - 0.8542T + 459.12)\mu$$

where O_2 is the amount of oxygen consumed (in standard cm^3/wafer), T is the process temperature (in °C), and μ is the thickness (in Å) of the thermal oxide film. Using this equation to predict the oxygen consumption for a 200-Å film for temperatures between 900 and 1050 °C results in a range of oxide consumption per wafer from 684 to 2904 standard cm^3/wafer (Figure 12).

Modules at the Process Flow Level. The fourth module type is based on the process flow for a particular product or

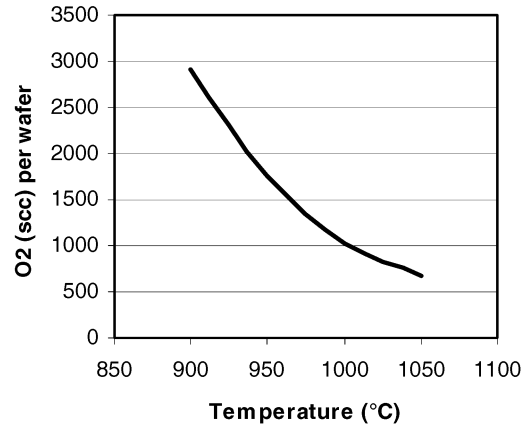

FIGURE 12. Oxygen consumption predicted as a function of process temperature in the furnace unit operation. The example shown is for a 200-Å thermal oxidation layer on an 8-in. wafer.

product type. Modules are developed using aggregated unit operation data that are generated by assuming an "average" function and recipe at each unit operation. This could be an actual average, as determined for a particular facility or as was the case in the example presented here, a single representative function and equipment type was selected as typifying each unit operation. The material and energy flows for each unit operation are estimated using a representative value; these values are then multiplied by the number of times the wafer is processed through the unit operation. Finally, the results are summed across the entire process flow.

To illustrate this method, an example is presented for energy consumption in a hypothetical facility manufacturing high-end microprocessors with either 6 or 8 layers of metal. The production line is divided into eight major unit operations with three subunit operations. The subunits are used when the unit operation involves functions that utilize very different pieces of equipment and consequently have different material and energy flows, such as in the photolithography unit operation where wafers are first coated with photo resist using a coater and then exposed using a stepper. Since the power requirements for each piece of equipment are different, it is useful to disaggregate the data in these particular instances.

A typical function and recipe through a typical piece of equipment is assumed for each unit operation. For example, in examining 30 furnace recipes representing 15 functions, throughput ranged from 28 to 60 wafers/h with both a mean and a mode of 34. Since all values of throughput for the purpose of this analysis were rounded to the nearest 5 wafers, 35 wafers/h is used for the furnace unit operation. The average power draw on a typical furnace at ISMT is 21 kW during processing and 16 kW during idle. Based on these values for power and assuming a throughput of 35 wafers/h, the energy consumed is calculated using the techniques described under "Modules at the Unit Operation Level".

The hypothetical wafer fabrication facility (fab) is assumed to be starting 5000 production wafers per week, operating 24 h a day, 7 days a week with an average 80% equipment availability or "up-time". In addition, it was assumed that there are an additional 500 (10%) test and monitor wafers being run. As in the comparison between the RTP and the vertical furnace above, throughput (wafers per hour) is used to determine total equipment demand time per week for a typical function in each unit operation using eq 1. This number is divided by the total available hours per week and rounded up to give the number of pieces of equipment to support the unit operation (eq 2). It should be noted that this assumes no dedicated pieces of equipment (i.e., any piece

TABLE 2. Average Number of Functions, Throughputs, and Power Requirements for a Hypothetical 0.13-μM Microprocessor Wafer Fab

unit operation	no. of functions: 8-layer metal	no. of functions: 6-layer metal	wafers/run	wafers/h	power (kW): process	power (kW): idle
implant	16	16	25	20	27	15
CVD	13	11	10	15	16	14
wafer clean	35	31	50	150	8	7.5
furnace	21	17	150	35	21	16
furnace (RTP)	7	7	1	10	48	45
photo (stepper)	27	23	1	60	115	48
photo (coater)	27	23	1	60	90	37
etch (pattern)	24	20	1	35	135	30
etch (ash)	27	23	1	20	1	0.8
metallization	11	9	1	25	150	83
CMP	18	14	1	25	29	8

of equipment can be used to run any function type within the unit operation). Since this is likely not the case, the numbers in our demonstration are probably lower than actual. The number of production hours is subtracted from the total available hours to estimate the amount of idle time (eq 3).

A process flow for a typical product is then defined, and the number of times a wafer is processed through each unit operation is accounted for. The values selected are intended to be typical for an 8-level and a 6-level metal 0.13-μm microprocessor and are given in Table 2 in columns 2 and 3, respectively. The average number of wafers run in a batch is given in column 4, and the average throughput in wafers per hour for an operation is listed in column 5. Power draws for both active and idle modes are given in the final two columns. The numbers in Table 2 are based on a variety of inputs from International SEMATECH as well as several member companies; they are intended to be representative values.

The inputs in Table 2 are used to estimate the amount of energy required to produce a 6-metal layer device as compared to an 8-metal layer device (Figure 13).

By parametrizing against the number of metal layers for a given product family and using relatively simple calculations, it can be estimated that the total energy required to fabricate an 8-layer metal device is 406 kW-h/wafer or 20% more than the 336 kW-h required to fabricate the same product with only 6 layers. The SIA road map (*11*) estimates that energy consumption related to fabrication equipment is approximately 0.7 kW-h/cm^2, which equates to 220 kW-h/8-in. wafer. While this number is significantly less than that estimated above, the numbers in the road map are intended to represent targets for "best-in-class" operations, not actual values, and it is known that the energy values included in the document are engineering estimates rather than the result of significant study (*12*). Williams et al. (*4*) provide data from three additional sources, all of which suggest a total energy demand of approximately 1.5 kW-h/cm^2 or 470 kW-h/8-in. wafer; however, none of the sources report values for equipment use only, so it is not simple to make a comparison. Energy consumption per wafer is provided in one other known publication, but the data are from an old facility running very small wafers and inputs from fabrication and infrastructure are combined; the value cited is 215 kW-h/wafer (*16*). Making adjustments for modern equipment, scaling to an 8-in. wafer, and excluding infrastructure, it is estimated that this would result in a value between 400 and 500 kW-h/8-in. wafer or higher than that predicted by the model.

In addition to determining the absolute amount of energy consumed, an important aspect of this type of analysis is the

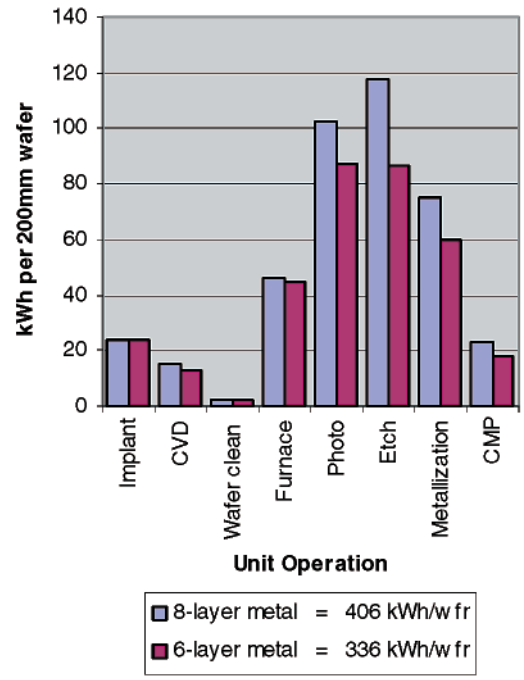

FIGURE 13. Comparison of the energy requirements for an 8-layer vs a 6-layer metal microprocessor indicates that the increase in energy is 70 kW-h/wafer or approximately 20%.

ability to estimate the relative effects that occur as the result of modifying a product design. The tradeoff analysis above identifies "etch" as the unit operation accounting for the largest increase in energy consumption in moving from 6 to 8 layers (30.8 kW-h/wafer). It is unlikely that it would be intuitive to either a process engineer or product designer that the addition of one layer-pair of metal would increase energy consumption per wafer by one-fifth. A manufacturing facility employing this methodology could also improve its understanding of energy and material flows and potentially identify opportunities to decrease consumption by focusing on those unit operations highlighted through use of a parametric module developed at the process flow level for a variety of product designs. Understanding of the drivers within the unit operation can be achieved by parametrization at the unit operation or function level as described above. Note that this example is for energy only and that materials may or may not scale similarly. It is also expected that the unit operations that are most affected will be different for different categories of materials. Water usage, for example, will almost certainly show the biggest increase in the wafer clean unit operation.

It should be noted that the above analysis is based on a mixture of process recipes, equipment specifications, and direct measurements on equipment to determine typical values. Direct and continuous monitoring of equipment would be required in order to obtain more precise values as well as the amount of variance. Gathering this type of data on an operating manufacturing line is potentially disruptive to product flow. Therefore, it is proposed that the primary purpose of such a model would be for tradeoff analyses to determine unit operations that are most critical overall. The etch operation in the example above appears to be the most significant in both the total amount and the relative increase in energy consumption. Ultimately, each wafer fabrication facility will need to develop its own data set for critical unit operations, but generic data sets could be used to help set priorities for further evaluations as well as to fill in gaps in the inventory with first order estimates.

TABLE 3. Current Content of the Energy and Material Database by Unit Operation[a]

	energy			water			elemental gases			specialty chemicals		
	E	*F*	*R*	*E*	*F*	*R*	*E*	*F*	*R*	*E*	*F*	*R*
implant	1	3		1	3		1	3		1	3	
CVD	3	12	53	1	2		1	2		1	2	
wafer clean	2	14	36	3	14	33	3	14	33	3	14	33
furnace	2	21	83				3	21	83	3	21	83
furnace (RTP)	1	7	5	1			1	2	2			
photo (stepper)	1											
photo (track)	1											
etch	1											
etch (ash)	1	3		1	3		1	3		1	3	
metallization	1											
CMP	1											

[a] Key to categories for which data has been collected: *E* = number of equipment types. *F* = number of functions. *R* = number of recipes.

Database

The data used to develop the examples described above are included in a database that is being used to generate a set of generic parametric material, energy, and emissions inventory modules for wafer fabrication. The focus has been on wafer clean and furnace unit operations. These operations are the most uniform across the industry in terms of equipment type, functions, and recipes; they are equally important for low-end products as well as high-end products; and they tend to have the least amount of proprietary data related to the use of specialty chemicals. For all these reasons they were considered to have the greatest potential for general application. They are also important operations in the overall accounting of energy and material flows for wafer fabrication.

Wafer clean is the unit operation with the greatest use of water, which as seen in Figure 4, represents by far the most significant mass flow in the manufacturing process. In addition, seven of the top eight specialty chemicals of interest listed in Table 1 are used in the wafer clean operation, six of them exclusively (isopropyl alcohol is used ubiquitously and tetramethylammonium hydroxide is used in photolithography). Nitrogen consumption in wafer clean is also extremely high, as it is used to dry the wafers at the end of the process. Energy is the only category that is not significantly impacted by the wafer clean operation; however, the energy required to create ultrapure water (UPW), while not addressed in this work, is very significant.

The furnace operation represents the fourth most intensive use of energy in the manufacturing of high-end products (Figure 13). In lower-end products (with fewer metal layers), it is likely to represent a larger portion of the overall energy use (note the relatively small change between 6- and 8-layer metal products). This operation also uses significant amounts of elemental gases, particularly nitrogen, oxygen, argon, and hydrogen.

The modules developed based on the database are expected to have applicability within a wafer fabrication facility for improvement of environmental performance or for insertion into life cycle assessment activities. Although it would be time-consuming, these data could be collected at any facility. In addition, equipment manufacturers are also beginning to recognize the importance of this information and are including energy and emissions data as part of equipment specifications. The type of data collected to date is indicated in Table 3. Six of the top eight specialty chemicals in Table 1 are included in the database. These are all used in the wafer clean operation. Energy measurements were taken directly on equipment at ISMT. Water, elemental gases, and specialty chemical use was determined from analysis of available recipes. Implant, ash, and RTP data are available through ISMT member confidential documentation. The remainder of the data is from personal communication with ISMT and two member companies and is proprietary. ISMT and one of the facilities represent high-end 8-in. wafer fabrication. Data from the second member facility represents a less aggressive suite of process and product designs from a 6-in. line. All of the data represent processes in use during the years 2001 and 2002.

Discussion

It has been estimated that approximately three-fourths of the fossil fuels and chemical inputs required to manufacture and use a semiconductor product, or microchip, is consumed during wafer fabrication. In addition, significant quantities of ultrapure water, amounting to at least four times the mass of fuel and materials used in semiconductor manufacture, are used (*2*, *4*). The total amounts of energy, materials, and water consumed in semiconductor manufacturing worldwide are also significant, highlighting the need to develop material and energy inventories for semiconductor device manufacture, both for use in improving environmental performance within the wafer fabrication facility and for use in life cycle assessment activities. There have been several barriers to the development of such inventories, including concern over protection of intellectual property and use of proprietary materials. However, the real challenge is the tremendous variability between products and facilities as well as very short product lifetimes (2 yr or less). This makes it nearly impossible to come up with a standard or even a few standard inventories for a semiconductor device.

This work has shown how even limited changes in the parameters of process and product design can result in significant changes in energy and material inventories. The parameters illustrated were layer thickness, the number of layers for roughly equivalent products, equipment type, production throughput, and process temperature. There are hundreds more, each which impact the use of energy, water, elemental gases, and specialty chemicals.

The proposed solution to facilitating development of inventories for wafer fabrication is to develop parametric modules based on unit operations, which change at a much slower rate than the product or process designs. In fact, the basic unit operations used to manufacture semiconductor devices have remained relatively unchanged for the past 30–45 yr, and the new ones are often adapted from other areas of electronics manufacturing (e.g., CMP from bare wafer polish and copper plated metallization from printed wiring boards). This approach is enabled by the fact that the industry is data-intensive. Much of the data are already available, and their use for development of inventory modules is dependent primarily on organization and analysis. In many cases, the relationships are based on fundamental physical and chemical properties and processes, and data can be collected that are relatively independent of the specific product being manufactured.

For material and energy inventory modules of the type described in this work to see widespread use, they must address issues of cost and yield. However, because the wafer fabrication process is extremely material and energy intensive, there are direct links between cost and energy and material consumption. Therefore, in addition to providing a framework for life cycle analysis inventory development, the methodology described here is consistent with cost of ownership models for economic optimization and facility design.

The purpose of this paper has been to introduce a framework and to illustrate the proposed methodology with a few examples. Further work is needed to address materials

flows and additional parametric relationships on the complete scope of unit operations for which data have been collected.

The parametric modules developed and described here are intended to support environmental analysis for wafer fabrication in the semiconductor industry. However, as micro- and nanotechnology-based manufacturing increase in importance on a global scale, it is important that we have methods available for the environmental analysis of complex and variable systems, particularly when they involve the production of emerging and therefore frequently changing technologies. The methodology proposed herein will facilitate effective application of the fourth principle of green chemistry in these economic sectors.

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